

Partial Order Relation



Introduction :- (Definition)

→ Any relation α on set (S) is called partial order relation if for any 3 arbitrary $a, b, c \in S$

relation have three types :-

1. R is reflexive

2. anti symmetric

3. R is transitive

• Reflexive relation :- aRa , or $a \leq a$

• Anti symmetric relation :- aRb & bRa $\Rightarrow a = b$ then $a \leq b$ or
 $b \leq a$ then $a = b$

• Transitive relation :- aRb & $bRc \Rightarrow aRc$
 $a \leq b$, $b \leq c \Rightarrow a \leq c$

Theorem:- The order relation less than equal to is partial order relation in Boolean algebra.

Proof of one:- reflexive relation.

For each $a \in B$, we have $a \cdot a' = 0$, this implies that $a \leq a$
Hence the relation \leq is reflexive.

(ii) Anti-symmetric relation:- Let $a, b \in B$ and $a \leq b, b \leq a$

and we know that:-

$$a, b \in B$$

$$a \leq b = a \cdot b' = 0 \quad \text{--- eq(i)}$$

$$b \leq a = b \cdot a' = 0 \quad \text{--- eq(ii)}$$

$$\begin{aligned} a &= a \cdot 1 \\ &= a \cdot (b + b') \quad [\text{By complementary law}] \end{aligned}$$

$$= a \cdot b + a \cdot b' \quad [\text{By distributive law}]$$

$$= a \cdot b + 0 \quad [\text{By using eq(i)}]$$

$$= a \cdot b$$

$$b = b \cdot 1 \quad [1 \text{ is multiplicative identity}]$$

$$b = b \cdot (a + a') \quad [\because a + a' = 1]$$

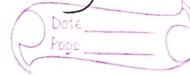
$$= b \cdot a + b \cdot a' \quad [\text{By distributive law}]$$

$$= b \cdot a + 0 \quad [\text{By using eq(ii)}]$$

$$= b \cdot a \quad [\text{By commutativity}]$$

$$= a \cdot b$$

$\therefore a \cdot 0 = 0$ is new law



(iii) Transitive relation:- Let $a, b, c \in B$ and $a \leq b, b \leq c$

$$a \leq b = a \cdot b' = 0 \quad \dots (i)$$

$$b \leq c = b \cdot c' = 0 \quad \dots (ii)$$

Now

$$\begin{aligned} a \cdot c' &= (a \cdot 1) \cdot c' \quad \rightarrow [\text{Identity law}] \\ &= a \cdot (b + b') \cdot c' \quad [\because 1 = b + b'] \\ &= a \cdot b + a \cdot b' \cdot c' \quad [\text{By distributive law}] \\ &= a \cdot b + 0 \cdot c' \quad [\text{By use of } i] \\ &= (a \cdot b) \cdot c' \quad [\text{By complementarity law}] \\ &= a \cdot (b \cdot c') \quad [\text{By associativity law}] \\ &= a \cdot 0 \quad [\text{By use eq(ii)}] \\ &= 0 \quad [\because a \cdot 0 = 0] \end{aligned}$$

Thus $a \leq b, b \leq c \Rightarrow a \cdot c' = 0$

$\Rightarrow a \leq c$

Hence the relation \leq is transitive.

Hence the order relation \leq is partial order relation.

Again

Theorem 3 :- (Homework) [denoted By $\sup^6(17)$]

* LEAST Upper Bound :-

Let $(B, +, \cdot, '')$ be a Boolean algebra. Let A be a subset of B . An element $b \in B$ is called an upper bound of A if and only if $a \leq b \forall a \in A$.

conditions :-

(a) c is an upper bound of the set A and

(b) $c \leq b$ for every upper bound b of A

* Greatest Lower Bound :- [denoted By $\inf(17)$]

Let $(B, +, \cdot, '')$ be a Boolean algebra. Let A be a subset of B . An element $b \in B$ is called a lower bound of A if and only if $b \leq a \forall a \in A$.

conditions :-

(a) c is a lower bound of the set A , and.

(b) $b \leq c$ for every lower bound b of A

Theorem :-

To prove that for any two elements a, b of a Boolean algebra:

(i) $a+b = \text{least upper bound of } a \text{ and } b$
 $a+b = \sup\{a, b\}$

(ii) $a \cdot b = \text{greatest lower bound of } a \text{ and } b$
 $a \cdot b = \inf\{a, b\}$

(i)

Proof :- Firstly we shall prove that $a+b$ is an upper bound of this set $\{a, b\}$.

So this will shall prove that

$$a \leq a+b \quad b \leq a+b \quad \left[\begin{array}{l} \therefore b = (a+b)' \\ a \cdot b' = 0 \end{array} \right]$$

$$\text{i.e., } a \cdot (a+b)' = 0$$

$$a \cdot (a' \cdot b') = 0$$

$$(a \cdot a') \cdot b' = 0 \quad [\text{By Associativity law}]$$

$$0 \cdot b' = 0 \quad [\because a \cdot a' = 0] \quad [\because 0 \cdot b' = 0]$$

0

Hence L.H.S prove R.H.S $[\because L.H.S = R.H.S]$

So, $a \cdot (a+b)' = 0$ or $a \leq (a+b)'$

i.e. $b \cdot (a+b)' = 0$

$$\begin{aligned} b \cdot (a' \cdot b') &= 0 \quad [\because \text{complementarity law}] \\ a' \cdot (b \cdot b') &\quad [\because \text{associativity law}] \\ a' \cdot 0 &\quad [\because b \cdot b' = 0] \quad [\because a' \cdot 0 = 0] \end{aligned}$$

0

$$= a' \cdot c' + b \cdot c' \quad [\text{By commutativity law}]$$

$$= 0 + 0$$

$$= 0$$

$$b \cdot c' = 0 \quad [\because (a+b) \cdot c' = 0 \Rightarrow a+b \leq c] \\ \text{lub } \{a, b\} = a+b.$$

Hence we prove

$$L.H.S = R.H.S$$

$$\text{So, } b \cdot (a+b)' = 0 = b \leq (a+b)$$

Ex :- If A, B is Boolean Algebra then

$$\exists u, y \geq z \Leftrightarrow u \geq z \text{ and } y \geq z$$

Thus from upation (1) and (2) it follows that $(a+b)$ is an upper bound of element A and B.

$$\begin{aligned} u \cdot y \geq z &\Leftrightarrow z \leq u \cdot y \\ u \geq z, y \geq z &\Leftrightarrow u \geq z, \text{ and } y \geq z \\ \text{we prove that } & \end{aligned}$$

Now we shall prove that $a+b$ is lub of a and b. and

suppose that r is also an lub of a and b. so

$$a \leq r, b \leq r$$

$$a \cdot r' = 0, b \cdot r' = 0$$

$$(a+b) \cdot r' = 0$$

Let

$$z \leq u \cdot y \Leftrightarrow z \leq u \text{ and } z \leq y$$

$$z \leq u \cdot y \text{ then }$$

$$z \leq u \cdot y, u \cdot y = \text{gib}(u, y)$$

$$z \leq u \cdot y, u \cdot y \leq u \text{ and } u \cdot y \leq y$$

$$z \leq u, z \leq y. \quad \dots \dots (1)$$

$$(a+b) \cdot c' = 0$$

$$c' \cdot (a+b) \quad [\text{By commutativity law}]$$

$$(c' \cdot a) + (c' \cdot b) \quad [\text{By distributive law}]$$

Chapter 5

Algebra of electric circuits:-

July conversely :-

Let $z \leq u$ and $z \leq y$ then

$$z \leq u \Rightarrow z+u = u \quad \text{(According to theorem no 13)}$$

$$z \leq y \Rightarrow z+y = y \quad [\text{as } a+b = b]$$

Now, $z+u \cdot y$

$$z+u \cdot y = (z+u) \cdot z+y$$

From eq(2) and (3)

$$z+u \cdot y = u \cdot y$$

$$z \leq u \cdot y \quad \text{--- (4)}$$

Hence from eq(1) and eq(4)

we have

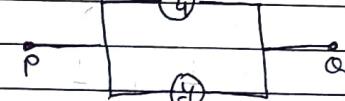
$$z \leq u \cdot y \Leftrightarrow z \leq u \text{ & } z \leq y$$

$$u \cdot y \geq z \Leftrightarrow u \geq z \text{ & } y \geq z$$

In parallel :-

when two switches u and y are connected

in parallel, then symbolically they are represented by the nation $u+y$.



$u+y \Leftrightarrow$ two switches u and y are connected in parallel.

In series :-

when two switches u and y are connected in series, then symbolically they are represented by the nation $u \cdot y$.



$u \cdot y \text{ or } uy \Leftrightarrow$ two switches u and y are connected in series.

Truth Table :- (In parallel) switching

when switch is u and y are connected in parallel

\Rightarrow	u	y	$u+y$
	1	1	01
	1	0	1
	0	1	1
	0	0	0

Relation between close and open switches:- If acts
represent the close switches then u will represent
an open switch conversely if u represents an open
switch then u will be
(a closed switch)

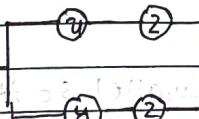


Truth Table:- (In series)

when switches u and y are connected in series

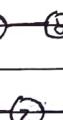
u	y	$u \cdot y$
1	1	1
1	0	0
0	1	0
0	0	0

(iv)



$$u \cdot z + y \cdot z$$

(v)

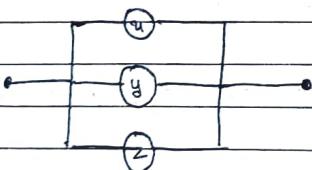


$$u \cdot y + z$$

* Switching circuit:-

Switching junction:-

Switching circuit



Switching function $f(u,y,z)$

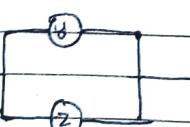
$$u \cdot y + z$$

(iii)



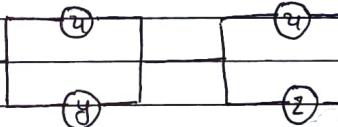
$$u \cdot y \cdot z$$

(iv)



$$u \cdot (y + z)$$

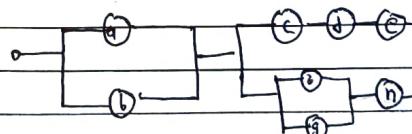
(vi)



$$u \cdot y \cdot w + u \cdot z$$

Ex:- 1. Find the switching net by switching function only polynomial

Q.S.



In word form:-

1. Switch a and b are connected in parallel. It is
represented by $(a+b)$

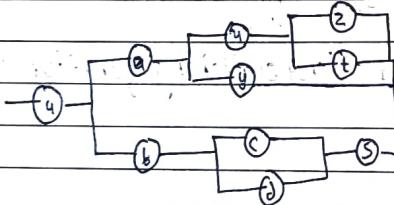
2. Switches c and d, e are connected in series which is represented by $(c \cdot d \cdot e)$

3. Switches f and g are connecting in parallel so it is represented by $(f+g)$. This system is connected in series with switch 'h' now it is represented by $(f+g) \cdot h$

Hence the given circuit is represented by the following polynomial.

$$[(a+b) \cdot (c \cdot d \cdot e) + (f+g) \cdot h]$$

Ques 7.



In word form:-

1. Switch a and b are connected in parallel. It is represented by $(a+b)$

3. Switch a is connected in series with u and y or the switch u and y are connected in parallel. It is represented by $a \cdot (u+y)$

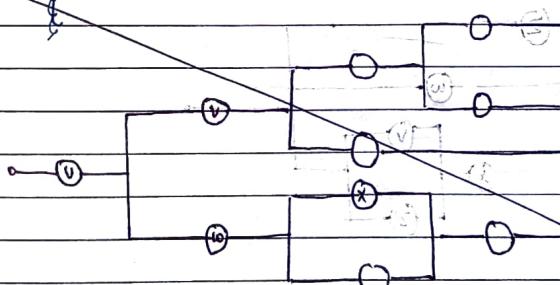
4. Switch u is connected in series with z and t and switch z and t are connected in ||. It is represented by $u \cdot (z+t)$

5. If switch b is connected in series with the switch c and d and switch c and d are connected in || or c and d are connected in s. b. $(c+d) \cdot s$

6. Directly all switches are series connect in u.

$$u \cdot [v \cdot (u \cdot (z+t) + y + w \cdot e \cdot u \cdot y) \cdot s]$$

Home work :-

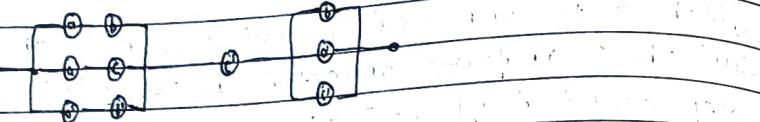


Homework:-

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6.



Soln:-

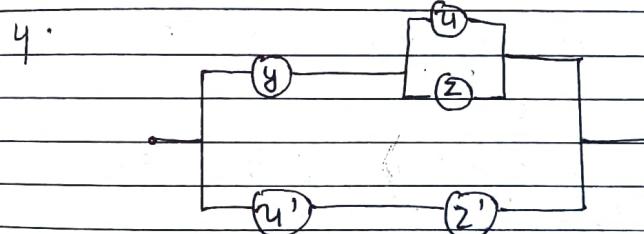
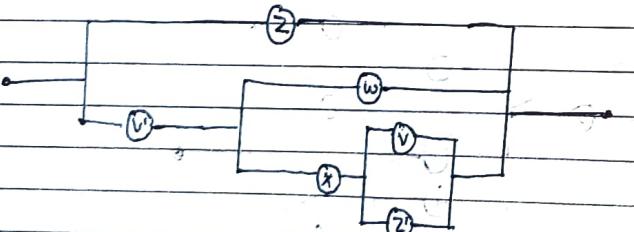
Ans:- (1) The first circuit clearly represented by the polynomial $(ab+a'b)$.

(2) The second circuit consists of which switch c' only. The third circuit is clearly represented by the polynomial $(b+a'+c')$.

(3) Since above three circuit are connected in series, hence the whole given circuit (6) is represented by the following polynomial:

$$[(ab+a \cdot a'b) \cdot c' \cdot (b+a'+c')]$$

8.



Soln:- Switches y and z are connected in parallel, which is denoted ytz .

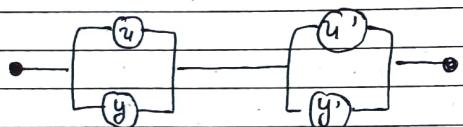
(iii) y and (utz) are connected in series which is denoted by $y(utz)$.

(iii) u' and z' are connected in series, which is denoted by $u'z'$.

(iv) Now $y|u+z|$ and $u'z'$ are connected in parallel, which is denoted by $y|u+z|+u'z'$.

$$[y|u+z| + u'z']$$

3.



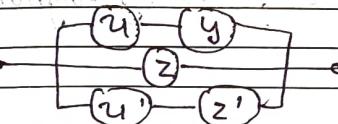
Soln :- (i) switches u and y are connected in parallel, which is denoted by uy .

(ii) switches u' and y' are connected in parallel, which is denoted by $u'y'$.

(iii) Now (uy) and $(u'y')$ are connected in series which is represented by $(uy)(u'y')$.

$$[(uy)(u'y')]$$

• 2.



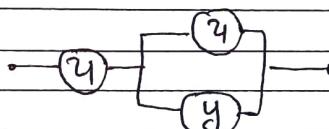
Soln :- (i) circuit u and y are connected in series, which is denoted by uy .

(ii) switches u' and y' are connected in series which is denoted by $u'y'$.

(iii) now uy, z and $u'y'$ are connected in parallel, which is represented by $uy+z+u'y'$.

$$[uy+z+u'y']$$

1.



Soln :- (i) switches u and y are connected in parallel and which is represented by uy .

(ii) This system is connected in series with switch y , which is represented by $y \cdot (uy)$.

$$[y \cdot (uy)]$$

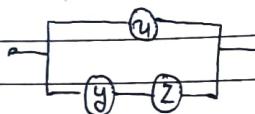
Ex :- 2 Design the circuits for the following polynomials:

(i) $u + yz$,

Soln :- switches u and yz are in parallel.

Switches y and z are in series.

Hence diagram of the given circuit

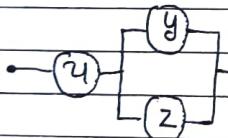


(ii) $u(y+z)$,

Soln :- (i) switches u and $y+z$ are in series while y and z are in parallel.

Hence diagram of the given circuit

(Ans)

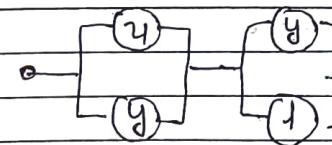


(iii) $(u+y)(z+1)$,

Soln :- the given net consists of two circuits in series
(i) first circuit is $u+y$, in which u and y are in parallel.

(iii) Second circuit is $z+1$ in which z and 1 are in parallel.

Hence diagram of the given circuit



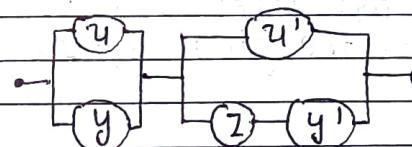
(iv) $(uy)(y'+zy')$

Soln :- (i) switch u and y are connected in parallel

(ii) switch u' and zy' are connected in parallel in while y and z are connected in series.

(iii) whole switch are connected in series.

Hence diagram of the given circuit.



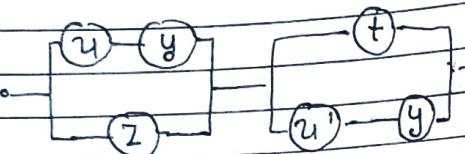
(v) $(uy+z)(t+u'y)$.

Soln :- (i) switches uy and z are connected in parallel in while u and y are connected in series

(ii) switch t and $u'y$ are connected in parallel in while u' and y are in series

(iii) whole circuit are in series

Hence diagram in the given below:-



(vi) $u(yz + yz)(sz + tw)$

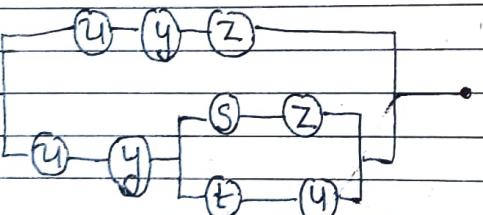
Soln:- Here switches u and y are connected in series.

(ii) switches ~~as~~ uy are series connected in $(sz + tw)$ and s and z are connected in series while t and w are connected in series.

(iii) s and z are parallel connected on tu .

(iv) whole circuit are connected in parallel.

Hence diagram of the given series.



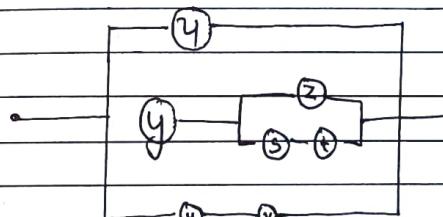
(vii) $u(ty)(z + st) + uv$

Soln:- (i) switch the u and y are connected in parallel and (ty) are series connected in $(z + st)$

(ii) z are parallelly connected in st and s t are connected in series.

(iii) v and v are connected in series and $(z + st)$ are parallelly connected on uv .

Hence diagram of the given circuit:-

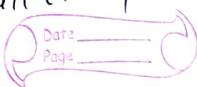


(viii) $u[y(z+w) + z(u+v)]$

Soln:- (i) first circuit is of u only.

(ii) second circuit is $y(z+w)$ in z and $(z+w)$ are connected in series while z and w are connected in parallel.

Homework :- all example:-



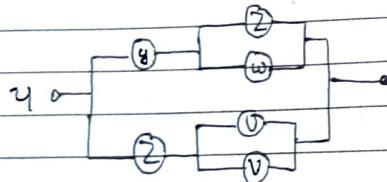
LOGIC GATES AND CIRCUITS:-



(iii) circuit $z(u+v)$ in which z and $u+v$ gate connected in series while u and v are connected in parallel.

(iv) circuit $y(u+w)$ and $z(u+v)$ gate in parallel and u is connected in series.

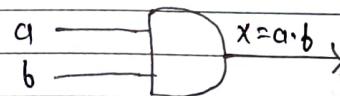
Hence diagram of the given below:-



Ex :- 3

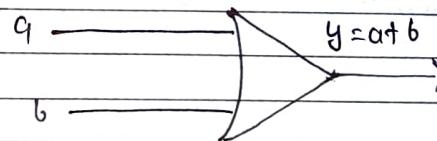
(i) AND-element or AND-gate:-

If there are two or more inputs then the output through the AND-gate (or AND-element) is a function of inputs and this function is obtained by the product of inputs.



(ii) OR-element or OR-gate:- If there are two or

More inputs then the output through the OR-gate is a function of inputs and this function is obtained by the addition of inputs.



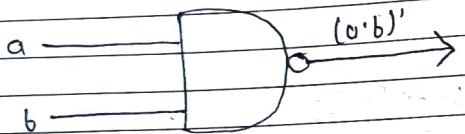
(iii) NOT-element or Inverter:-

Not element changes the input to the complement of it i.e. the output through the NOT-element is the complement of input.

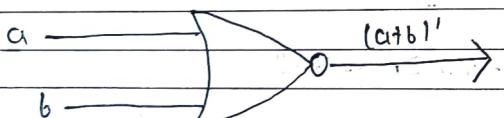


Combination of gates:-

1. AND-NAND gate:- It is equivalent to AND gate followed by NOT gate if A and B are two inputs then output is NAND gate is $(a \cdot b)'$.



2. NOR-gate:- It is equivalent to an OR-gate followed by a NOT-gate if a and b are two inputs then output-they output NOR-gate is $(a+b)'$.



Truth Table of NAND Gates:-

a	b	$(a \cdot b)$	$(a \cdot b)'$
1	1	1	0
1	0	0	1
0	1	0	1
0	0	0	1

Truth Table of NOR Gates:-

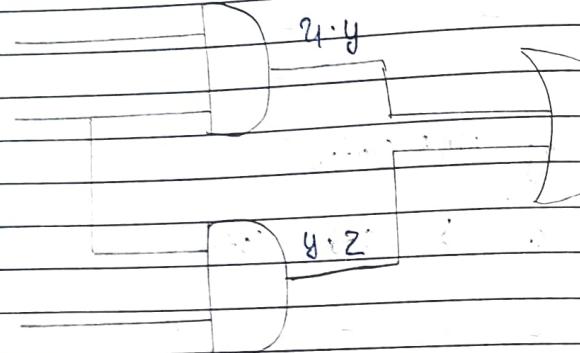
a	b	$(a+b)$	$(a+b)'$
1	1	1	0
1	0	1	0
0	1	1	0
0	0	0	1

Hw

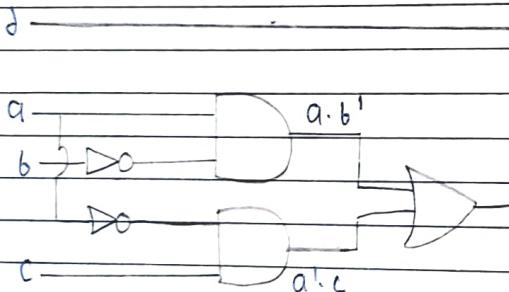
Ex :- 1 Draw the logic circuit for each of the following Boolean expressions:

$$(ii) u = y \cdot z$$

Solⁿ :-



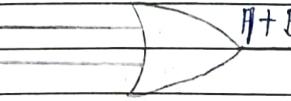
$$(iii) d \cdot (a \cdot b' + a' \cdot c)$$



$$(iv) u = (A+B) \cdot C$$

Solⁿ :- A

B



$$(iv) x = A(B+C+D)$$

Solⁿ :-

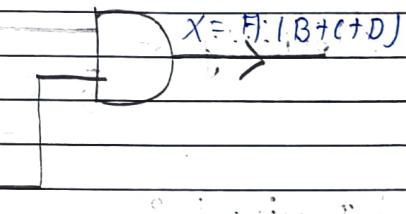
A

B

C

D

$$x = A \cdot (B+C+D)$$



Homework :- Theorem :-

The set $\{f_n\}$ of all switching functions of n variables forms a Boolean algebra with respect to operations '+', '!', and '•'. In other words, the following postulates hold for all $f, g, h \in \{f_n\}$

(ii) Commutativity :-

$$f \cdot g = g \cdot f$$

(iii) Associativity :-

$$(f + g) + h = f + (g + h)$$

$$(f \cdot g) \cdot h = f \cdot (g \cdot h)$$

(iv) Distributive :-

$$f(g + h) = fg + fh$$

$$f + gh = (f + g)(f + h)$$

(v) Identity :-

$$f + 0 = f$$

$$f \cdot 1 = f$$

(vi) Domiant :-

$$f + 1 = 1$$

$$f \cdot 0 = 0$$

(vii) Idempotent :-

$$f + f = f$$

$$f \cdot f = f$$

(viii) Complementation :-

$$f + f' = 1$$

$$f \cdot f' = 0$$

(viii) De-Morgan's law :-

$$(f + g)' = f' \cdot g'$$

$$(f \cdot g)' = f' + g'$$

(ix) Involution :-

$$(f')' = f$$

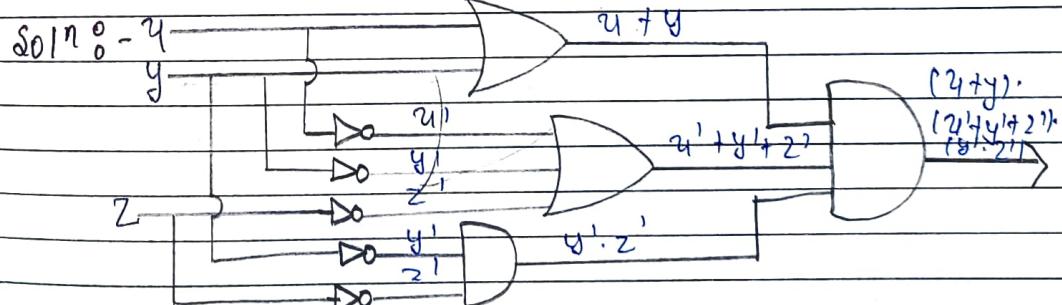
(x) Absorption :-

$$f + fg = f$$

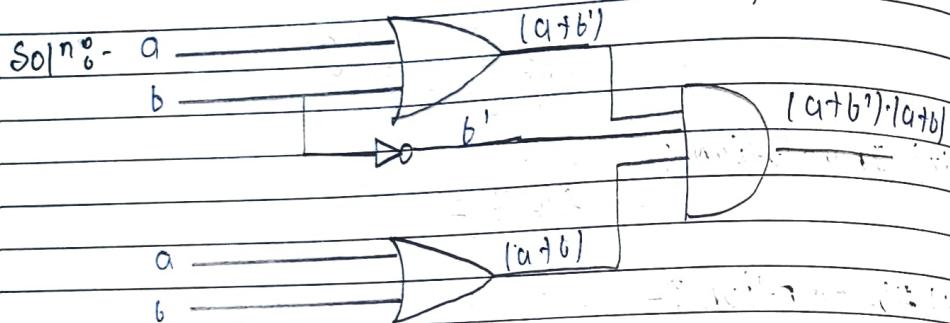
$$f \cdot (f+g) = f$$

Ex :- 2 Draw the logic circuit for each of the following expression :-

$$(i) (u + y) \cdot (u' + y' + z') \cdot (y' + z')$$

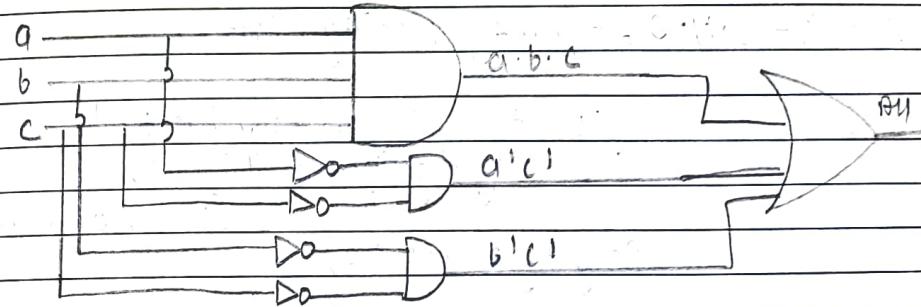


(ii) $(a+b') \cdot (a+b)$



Ex^o-4 $x = abc + a'b'c' + b'b'c'$

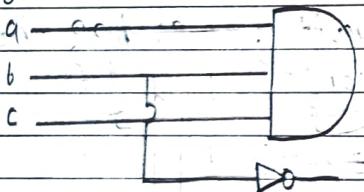
Solⁿ-



Ex^o-3

(iii) $y = ab'c + abc' + ab'b'$

Solⁿ-



prove the following Boolean identities:-

(i) $(u'y+z)'(u'+z)' + (u'y+z)(u'+z) = u+y+z$

Solⁿ- L.H.S - $((u'y+z)' + (u'+z))(u'+z)' + (u'y+z)$
 $((u'y)'z' + u'+z)(u+z' + u'y+z)$
 $((u+y')z' + u'+z)(u+z' + u'y+z)$
 $(u+z'+z) + (y'z + u)(u'y)$
 $u+z + y'z + u'y + uu'y$
 $u+z + y'z + z$
 $(z+u+z+u')(z+u+z+y)$
 $(z+u'+u)(z+u'+z)(z+u+y)(z+u+y)$
 $(z+1)(1+u')(u+y+z)(1+y)$
 $1 \cdot 1(u+y+z) \cdot 1$
 $u+y+z.$

HOMEWORK:-

$$(ii) (y+y')(y'+y)(y+z) = y+y+z(y+y')(y'+y)(y+z)$$

$$\text{Soln} :- L.H.S - (y+y')(y'+y)(y+z)$$

$$(y'y + y'y + y'y' + yy')/y+z \\ (0 + yy' + y'y + 0)/y+z$$

$$[yy + y'y]/y+z$$

$$yy + y'y + zyy + zy'y$$

$$yy + y'y + zyy + zy'y$$

$$yy(y+z) + y'y(y+z)$$

$$yy(y+z) + y'y(y+z)$$

$$(y+y')(y'+y)(y+z)$$

Ex :- 3

Solve the following switching functions, draw a simple switching circuit:

$$(i) f(y, y) = y + y \cdot y$$

$$\text{Soln} :- f(y, y) = y + y \cdot y$$

$$= y \cdot 1 + y \cdot y$$

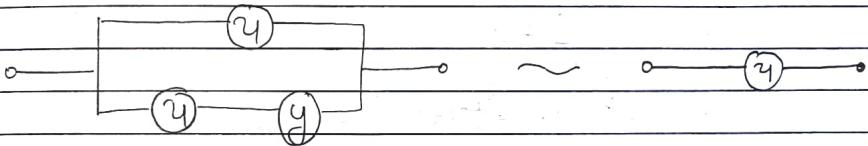
$$= y \cdot (1+y)$$

$$= y \cdot (y+1)$$

$$= y \cdot 1$$

$$= y$$

$$(y+1) = 1$$



$$(ii) f(y, y) = y \cdot y' + y \cdot y$$

Soln :-

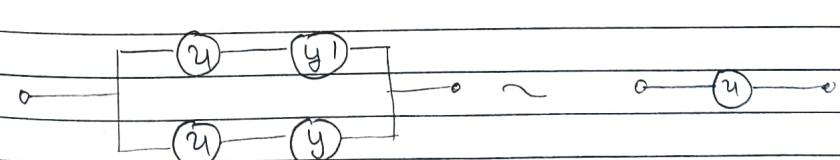
$$y \cdot y' + y \cdot y$$

$$y(y' \cdot y)$$

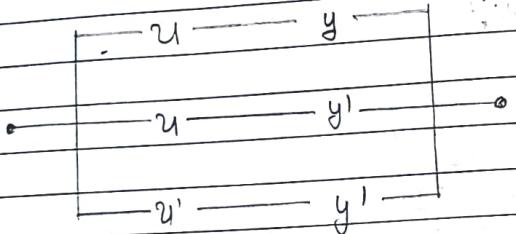
$$y \cdot 1$$

$$y$$

$$[y' \cdot 1 = 1]$$

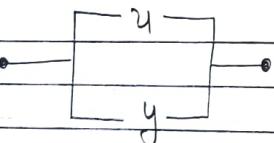


Ex :- Draw a simple circuit for the following diagram and verify the equivalent circuit by truth table verification by truth tables.



$$\text{Soln:- } f(y, u) = (u \cdot y) + (u \cdot y') + (u' \cdot y)$$

$$\begin{aligned}
 &= u \cdot (y + y') + (u' \cdot y) \\
 &= u \cdot 1 + u' \cdot y \quad [\because u \cdot 1 = u] \\
 &= u + u' \cdot y \\
 &= (u + u') \cdot (u + y) \quad [\because u + u' = 1] \\
 &= 1 \cdot (u + y) \\
 &= u + y
 \end{aligned}$$



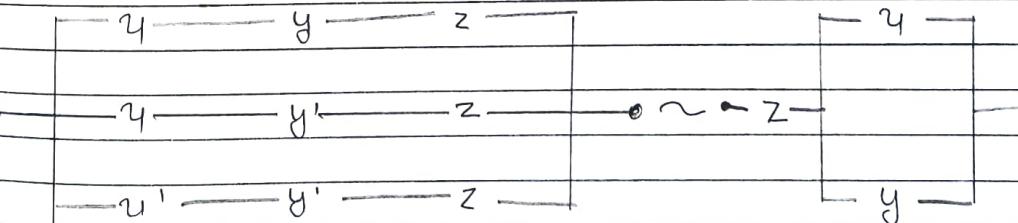
Truth table:

u	y	u · y	y'	u' · y'	u · y + u' · y'	u' · y + u · y'	u · y + u' · y + u' · y'
1	1	1	0	0	0	1	1
1	0	0	1	1	0	1	1
0	1	0	0	0	1	0	0
0	0	0	1	0	1	1	1

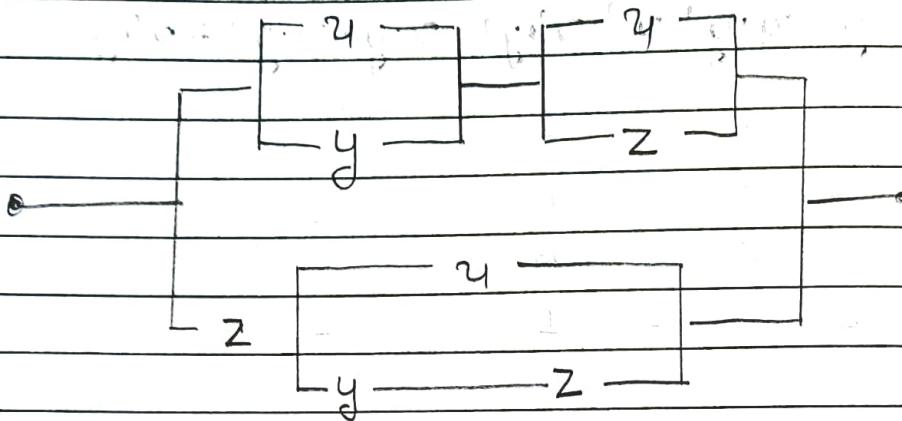
Ex :- Replace the switching function by a simple switching circuit.

$$f(u, y, z) = u \cdot y \cdot z + u \cdot y' \cdot z + u' \cdot y \cdot z$$

$$\begin{aligned}
 \text{Soln:- } f(u, y, z) &= u \cdot y \cdot z + u \cdot y' \cdot z + u' \cdot y \cdot z \\
 &= (u \cdot y + u \cdot y' + u' \cdot y) \cdot z = z \cdot [u \cdot (y + y') + u' \cdot y] \\
 &= z \cdot [u \cdot 1 + u' \cdot y] = z \cdot [u + u' \cdot y] \\
 &= z \cdot (u + u' \cdot (u + y')) = z \cdot (1 \cdot (u + y')) = z \cdot (u + y') \\
 &= z \cdot (u + y')
 \end{aligned}$$



Ex :- Replace the following switching circuit by a simple one



$$\begin{aligned}
 \text{SOLN:- } f(u, y, z) &= (u \cdot y) \cdot (u + z) + z \cdot (u + y \cdot z) \\
 &= u \cdot y \cdot z + z + (u + y \cdot z) \\
 &= (u + y \cdot z) \cdot 1 + z \cdot (u + y \cdot z) \\
 &= (u + y \cdot z) \cdot (1 + z) \\
 &= (u + y \cdot z) \cdot 1 \\
 &= u + y \cdot z
 \end{aligned}$$